REMARKS

Claims 1-7 were pending in the present application. By virtue of this response, claim 1 has been amended. Accordingly, claims 1-7 are currently under consideration. Amendment and cancellation of certain claims is not to be construed as a dedication to the public of any of the subject matter of the claims as previously presented. No new matter has been added.

Rejections under 35 U.S.C. §102(e)

The Office has rejected claims 1 and 6 as allegedly being anticipated by Uchida et al. (U.S. Patent No. 6,636,444, hereinafter the Uchida reference). Applicant respectfully traverses this rejection as it applies to the amended claims.

Applicant submits that the Uchida reference fails to disclose each and every element recited in the independent claim 1. In particular, the Uchida reference fails to disclose at least the elements of 1) data from the page buffer is processed for prohibiting unnecessary data from being written into the plurality of memory cells; and 2) a masking section for masking at least a portion of data read from the page buffer section based on a characteristic of a particular write operation regarding that data. The Uchida reference teaches a method for solving the problem of the Delayed Write technique, which is commonly employed in synchronous dynamic random access memories (SDRAMs). According to the Uchida reference, the method provides "a semiconductor memory device in which data transfer rate is increased without having to provide a register for holding write data." (see Uchida, column 1, lines 53-56) This goal is accomplished by separating the read data line and the write data line from each other within the memory core.

The present invention describes a semiconductor memory device which can be controlled so that certain data temporarily buffered in a page buffer circuit, is prohibited from being written into the memory cells. According to one embodiment of the present invention, when transferring data from the page buffer to the memory cells in the byte mode, the unnecessary bytes of a word will be masked (see Figures 4A to 4C). As a result, the control circuit is simplified and the performance of the memory device is improved. However, the Uchida reference does not teach

or suggest this aspect of the invention for prohibiting unnecessary data from being written into the memory cells.

In addition, although the Uchida reference discloses a mask signal, it does not teach or disclose how the mask signal is used masking data based on a characteristic of a particular write operation, such as the bus width of the data. In the Office Action, the Examiner contends that "Figures 8A and 8B of Uchida discloses a portion of masking data is based on a characteristic of a particular write operation regarding that data." The Applicant respectively submits that the mask signal "MASKZ" in Figures 8A and 8B of Uchida is inactive throughout the read and the write operations. Even if the 1 bit MASKZ signal is active as cited by the Examiner (see Uchida, column 10, lines 23-29), the MASKZ signal may be able to disable the transfer of a fixed bus width of data to the memory cells. It is impossible for the 1 bit MASKZ signal to mask different portions (multiple bits) within a word. Thus, the Uchida reference does not disclose each and every element of claim 1. It is respectfully submitted that the independent claim 1 and its dependent claims 2-7 are allowable over the Uchida reference.

Rejections under 35 U.S.C. §103(a)

The Office has rejected claim 7, as allegedly being unpatentable over Uchida et al. (6,636,444 B2) in view of Applicant Admitted Prior Art. For the reasons presented above, since the Uchida reference does not anticipate each and every element of claim 1, which claim 7 depends from, claim 7 can not be found obvious over Uchida in view of Applicant Admitted Prior Art.

In addition, the Uchida reference teaches away from the use of the page buffer of the present invention. According to the Background and Summary sections of the Uchida reference, the Data I/O Buffer Register, which the Examiner contends to be equivalent to the page buffer of the present invention, "not only leads to increased chip area, but also becomes a factor that increases the cost." As a result, the Uchida reference attempts to increase the data transfer rate "without having to provide a register for holding write data." (see Uchida, column 1, lines 40-42 and 53-56) Therefore, it is improper to combine the Uchida reference and the Applicant Admitted Prior Art.

CONCLUSION

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue. If it is determined that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

In the event the U.S. Patent and Trademark office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to Deposit Account No. 03-1952 referencing docket no. 299002056600. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

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Respectfully submitted,

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